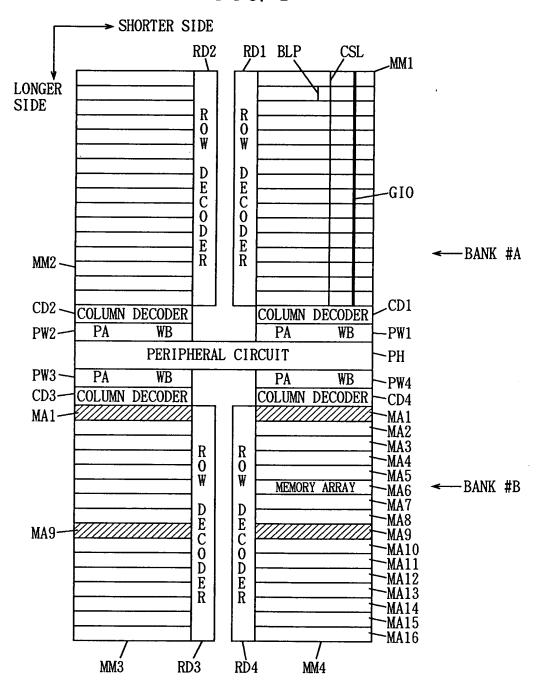
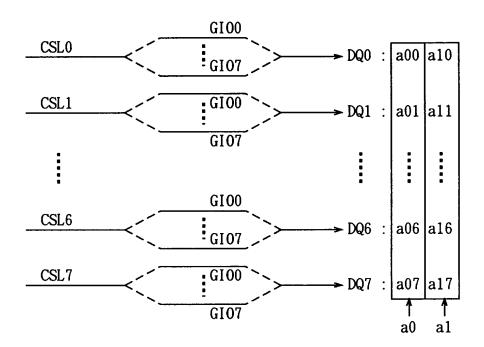
F I G. 1

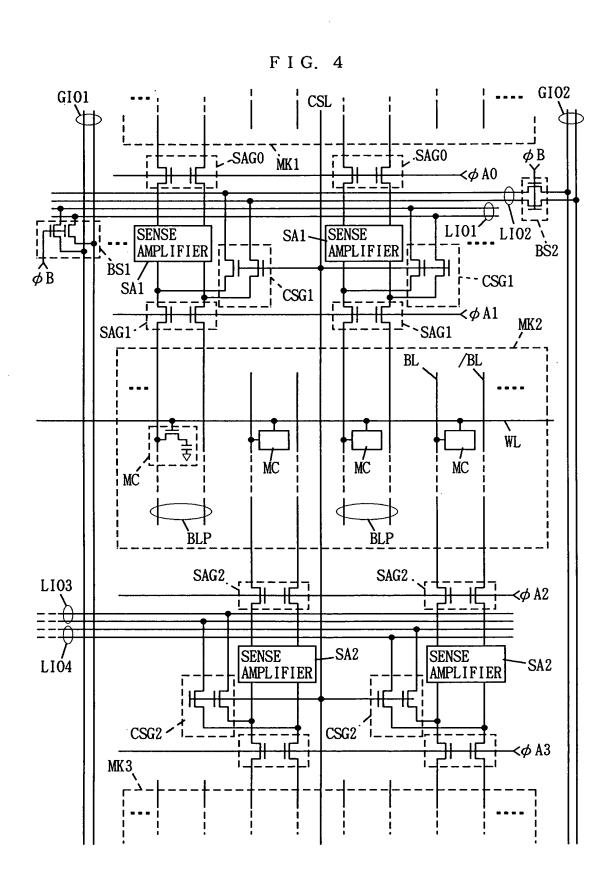


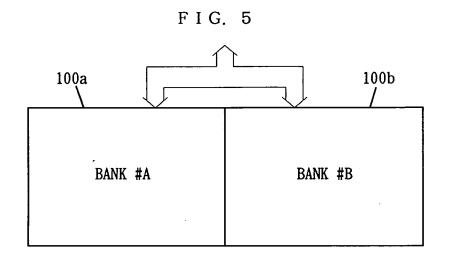
3/1/

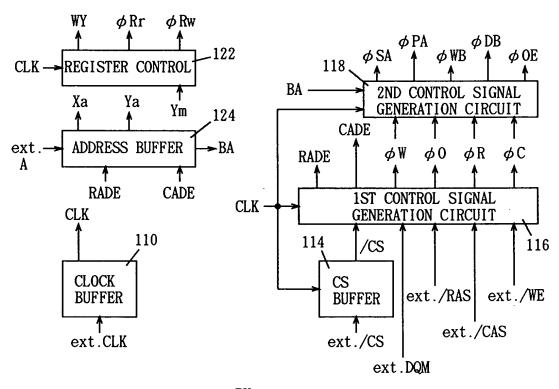
F I G. 2 MSA1 WS MSA2 MA AG1 AG2 8 9 10 11 12 13 14 15 16 AG3 AG4 MK BLP GIO BS BS MK 32-KILO BIT CSL AG1 8 GLOBAL IO LINE PAIRS WS CSL AG2 8 GLOBAL 10 LINE PAIRS WS CSL AG3 8 GLOBAL IO LINE PAIRS WS -CSL AG4 8 GLOBAL IO LINE PAIRS rio rio GĬO

F I G. 3









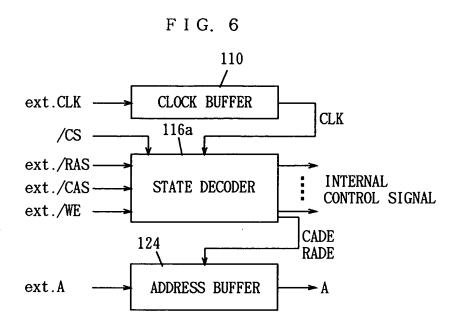
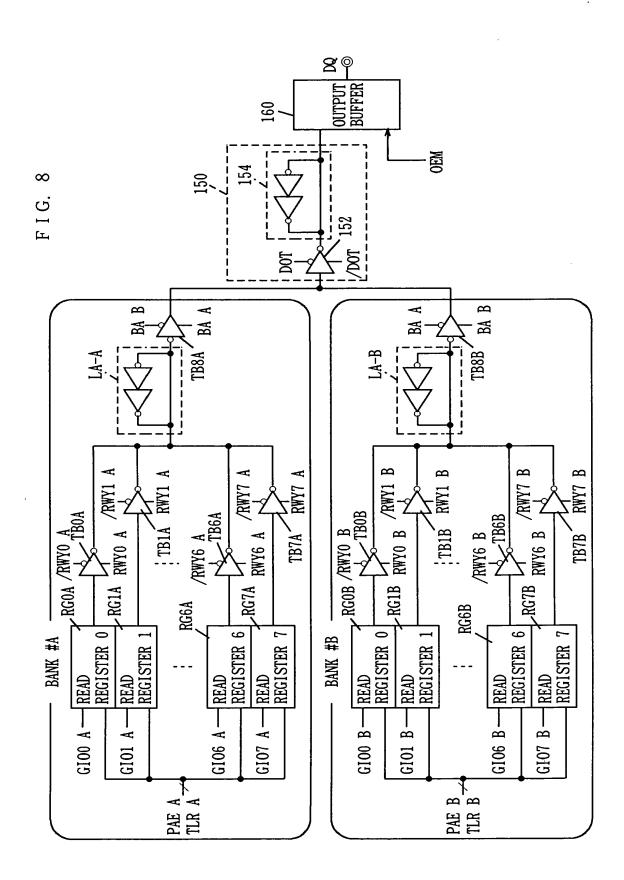
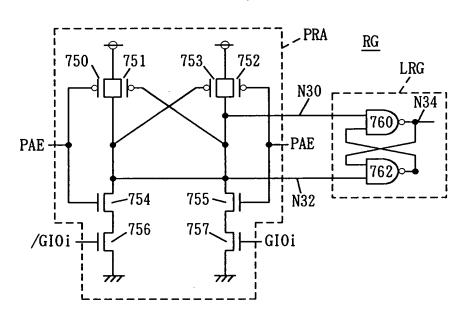


FIG 7

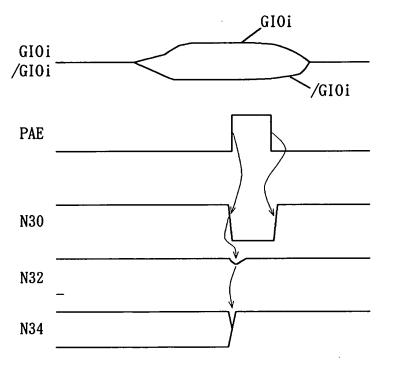
FUNCTION	SD/	/RAS	/CAS /WE	/WE	MOQ
ROW ADDRESS STROBE AND ARRAY ACTIVATION	Г	Т	Н	Н	
COLUMN ADDRESS STROBE AND READ	L	Н	Т	Н	1
COLUMN ADDRESS STROBE AND WRITE	L	Н	Т	L	_
PRECHARGE / SELF REFRESH END	L	L	Н	L	
REFRESH / SELF REFRESH START	L	L	Г	Н	_
SET MODE REGISTER	L	L	L	Г	****
WRITE ENABLE / OUTPUT ENABLE	_	-	_	_	7
WRITE MASK / OUTPUT DISABLE	-	1	ı	-	Н
NO CHANGE	L	Н	Н	Н	-
IGNORE /RAS, /CAS & /WE	Н	×	×	×	l

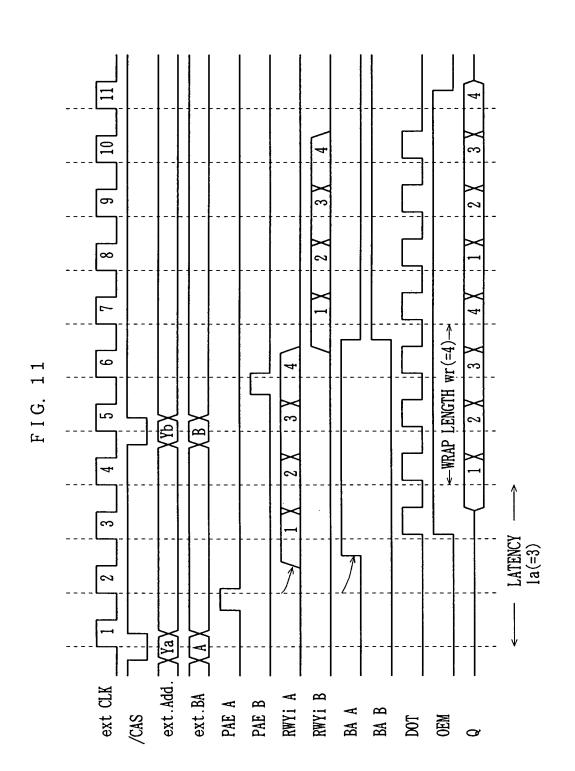


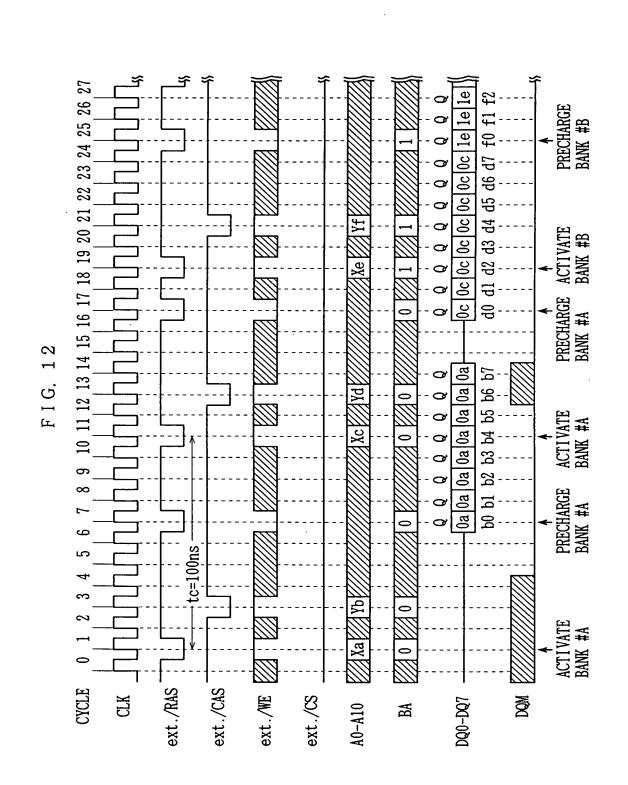
F I G. 9

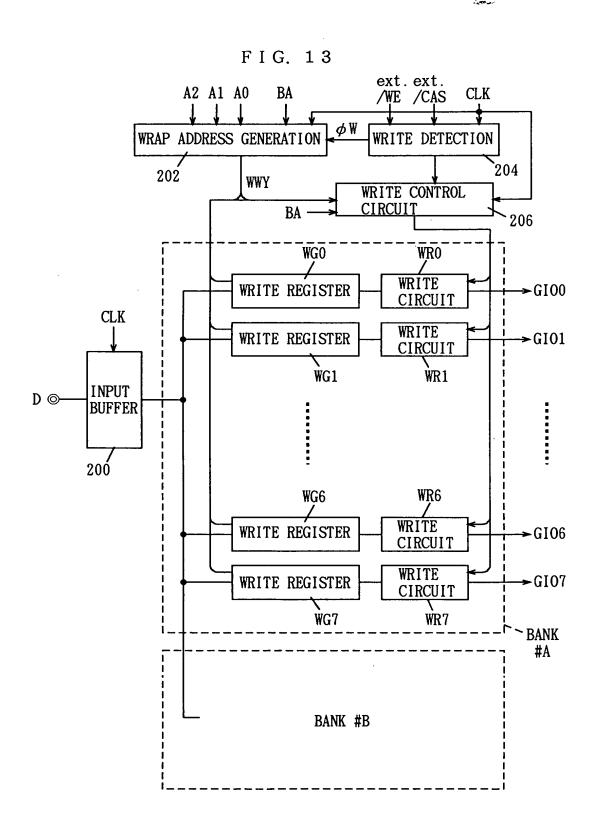


F I G. 10



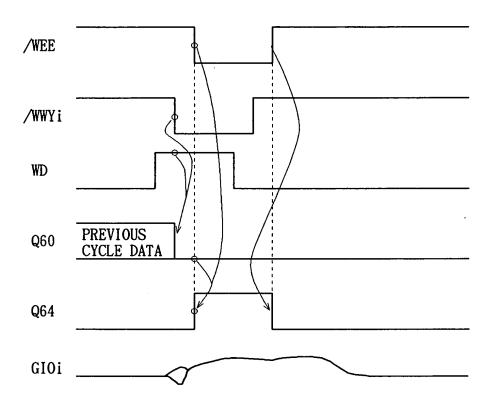


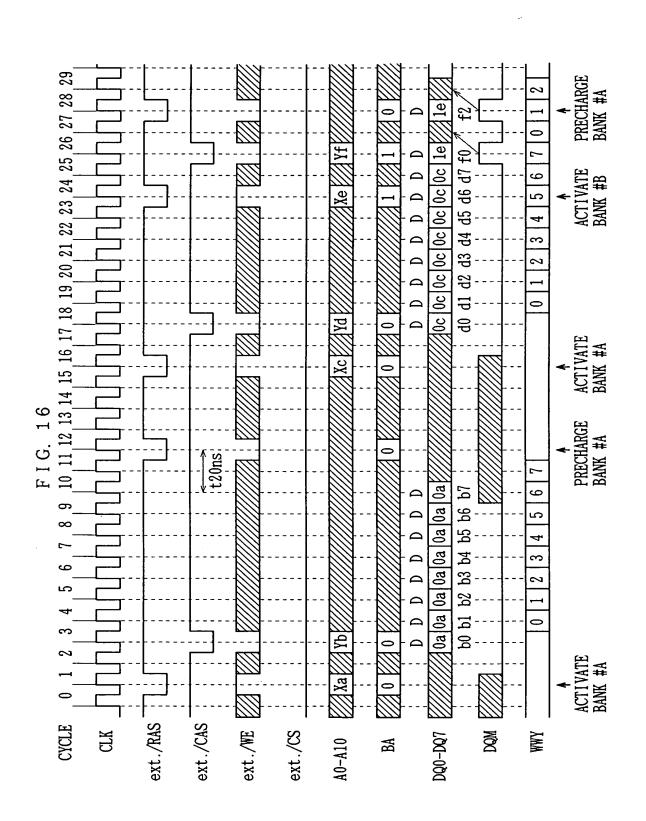


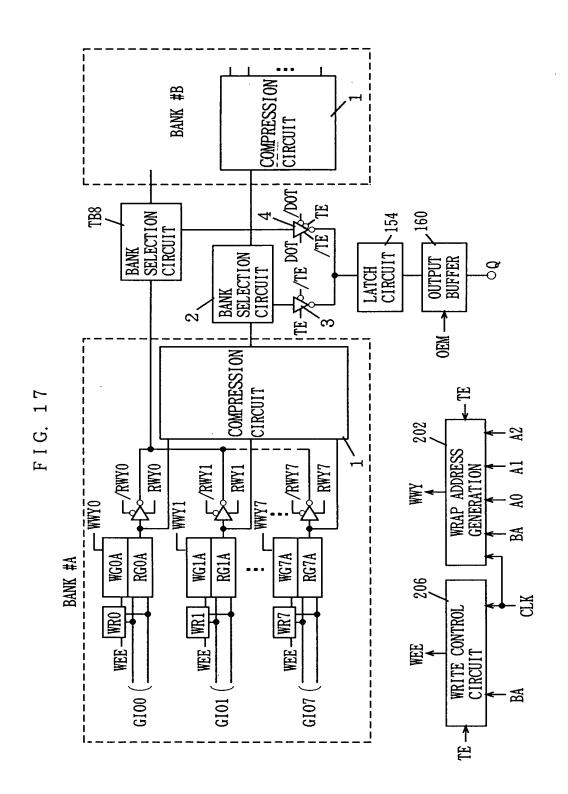


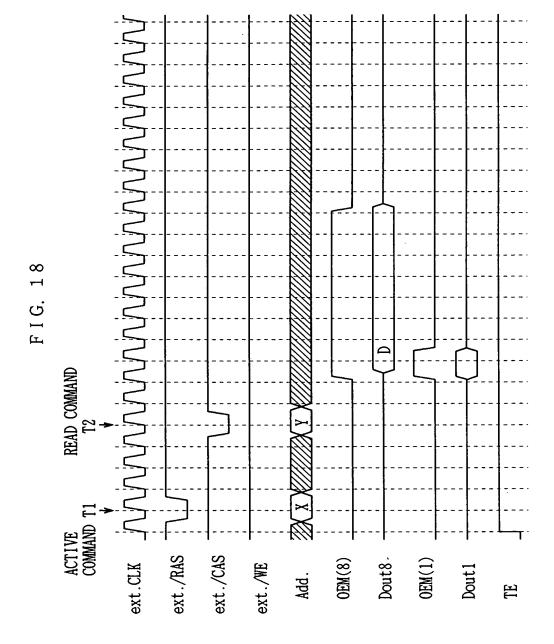
MR. 065 064 FIG. 14 250 233 P

FIG. 15









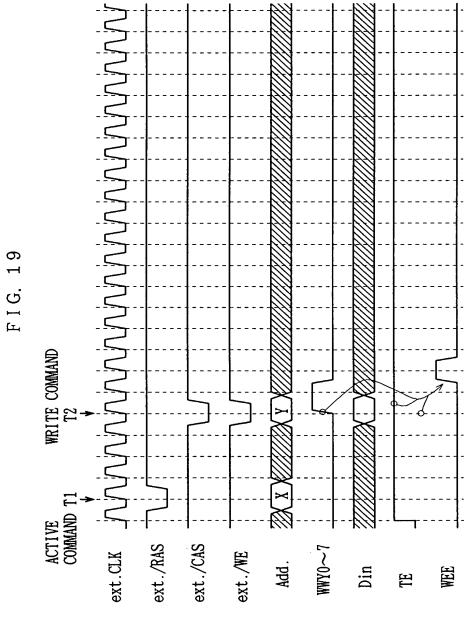
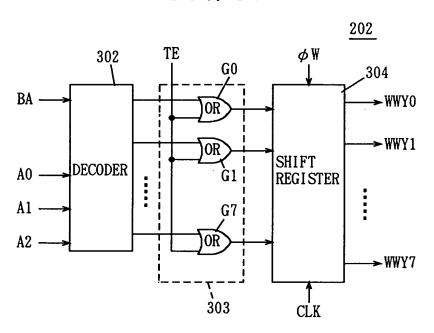
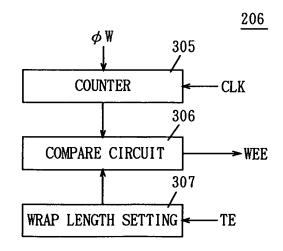
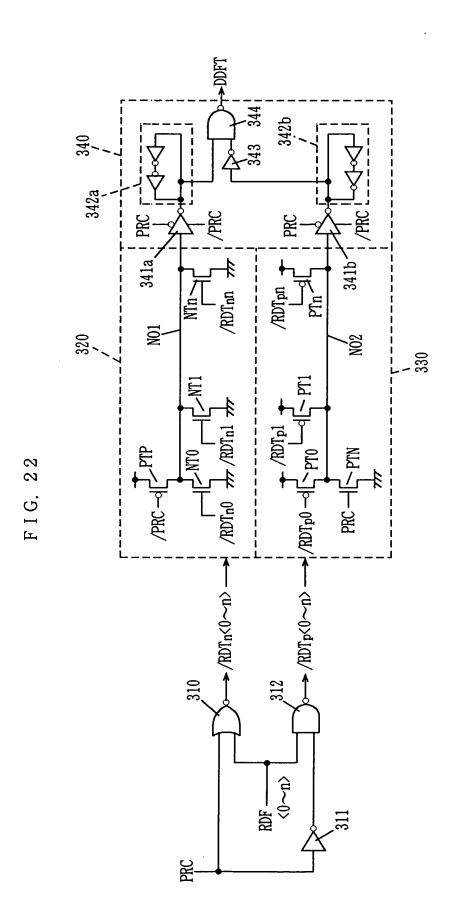


FIG. 20

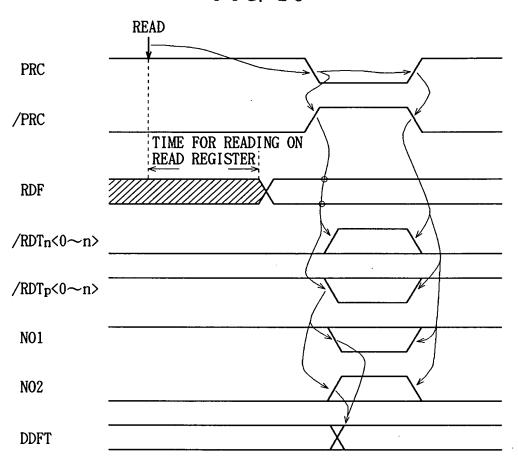


F I G. 21





F I G. 23



F I G. 24

	/RDT N/P <0:7>	NO1	NO2	DDFT	DECISION
PRECHARGE	L/H	Н	L	-	-
ALL "H"	L	Н	Н	H	PASS
ALL "L"	Н	L	L	Н	
"H" AND "L"	H & L	L	Н	L	FAIL

FIG. 25

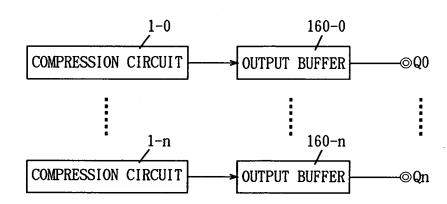
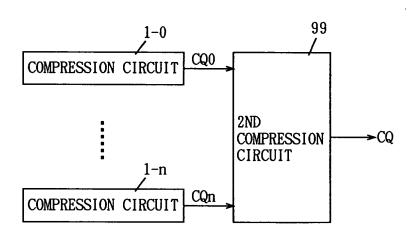
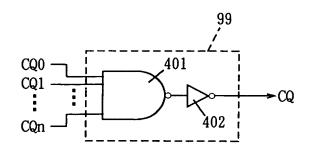


FIG. 26



F I G. 27



F I G. 28

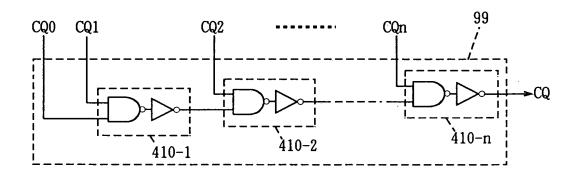
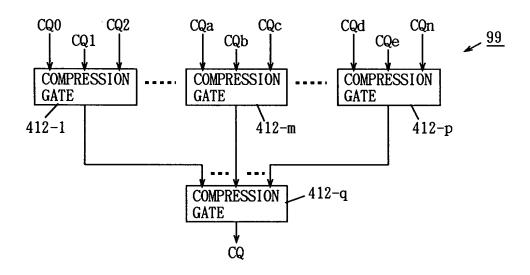


FIG. 29



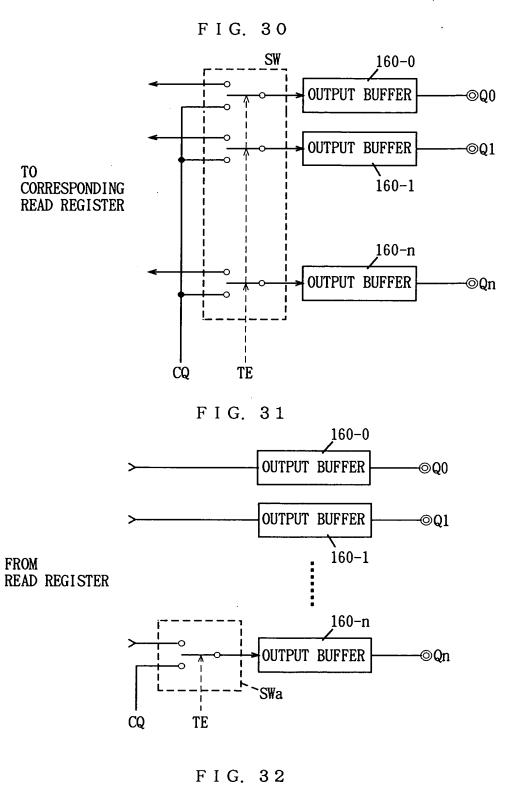
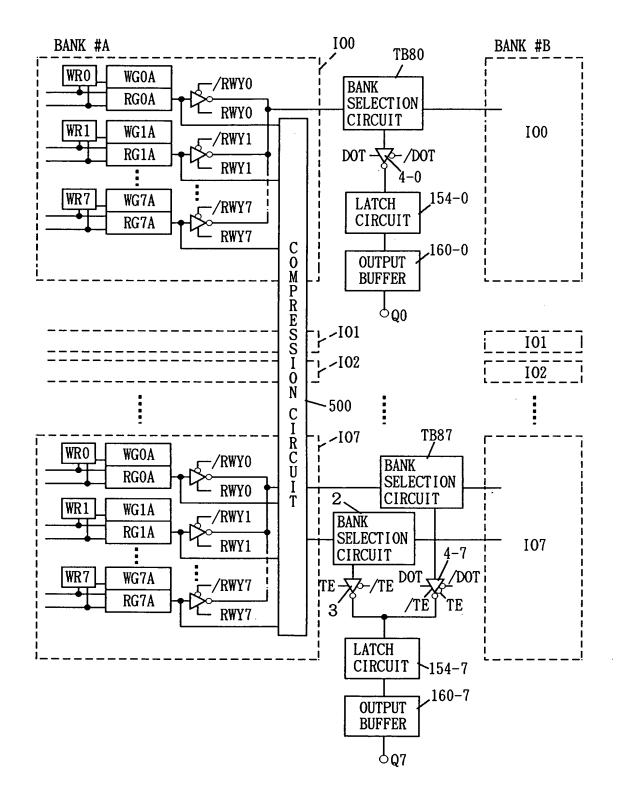


FIG. 33



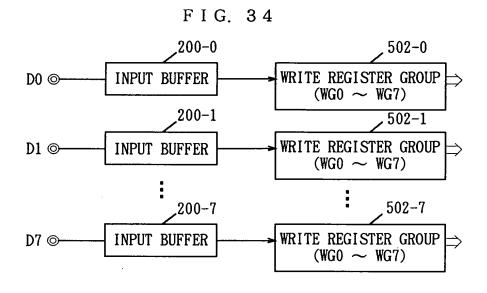
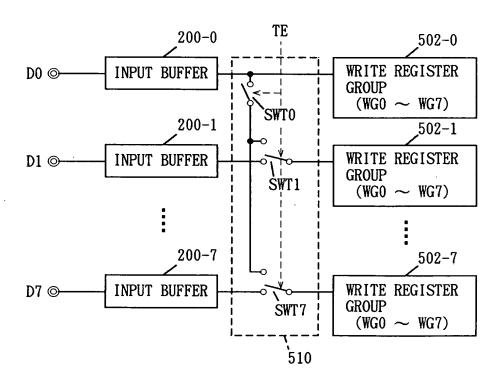


FIG. 35



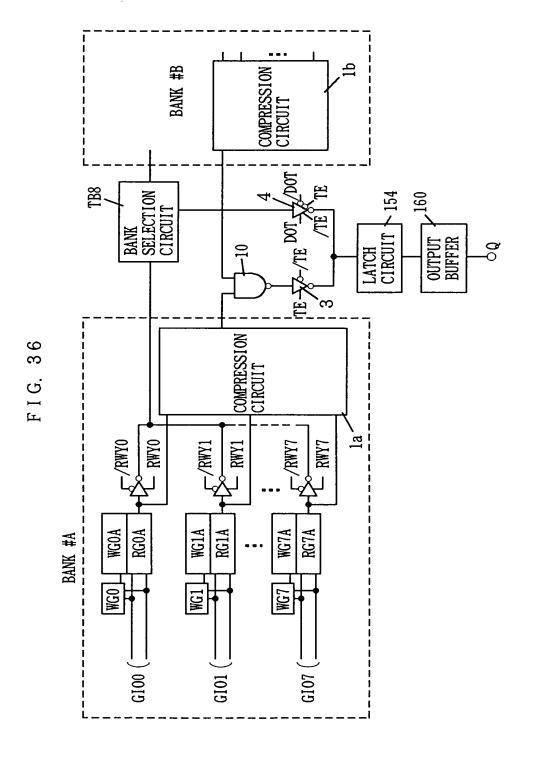


FIG. 37

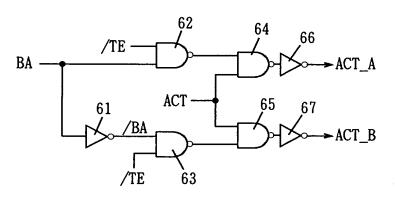
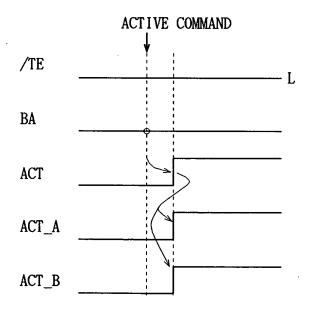


FIG. 38



F I G. 39

